## REMARKS/ARGUMENTS

In the Office action dated August 24, 2005, the Examiner rejected claims 1, 2, 4, 5, 8, 10 - 12, 15, 16 and 19 - 21 under 35 U.S.C. § 103. Claims 3, 6, 7, 9, 13, 14, 17, 18, 22 and 23 were deemed allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

By this Amendment, Applicant has amended claims 1, 3, 7 - 9, 11, 15, 17 - 19, 22 and 23 and added claims 24 - 37. Reconsideration of claims 1 - 37 that are now pending is hereby requested.

### Allowable Claims

Claims 3, 7, 9, 17, 18, 22 and 23 have been amended to independent form. Accordingly, Applicant submits that these claims are in condition for allowance.

### Response to the Rejection of Claims 1, 2, 4, 5, 8, 10 and 11

Claims 1, 2, 4, 5, 8, 10 and 11 were rejected under 35 U.S.C. § 102(b) as being obvious in view of Popescu, U.S. Patent Application No. 5,432,480 (referred to hereafter as "Popescu"). Claims 1, 8 and 10 are independent.

Popescu discloses in Figure 1 a conventional Hogge-type linear phase detector. Here a clock signal (CLK) drives a pair of flip flops 112 and 113 to latch a data input signal (DIN). In accordance with conventional practice, the CLK signal is of a higher frequency than the DIN signal so that all of the transitions of the DIN signal may be sampled.

As shown in Figure 2 of Popescu, all of the flip flops are of the same speed. Namely, both inputs (DIN and DOUT) to the flips flops 112 and 113 are of the same frequency. See also column 3, lines 59 - 66 ("The second flip flops retimes the retimed data signal DOUT . . . to generate a twice-retimed data signal DT.").

The CLK signal is generated by delaying (via element 222) the output of the VCO 120. Here, Popescu takes advantage of the symmetric characteristic of the CLK signal. That is, by imparting an appropriate delay, the CLK signal may be set such that "the clock edge is centered in the data eye" (column 7, lines 14 - 25). This is possible because each clock edge is evenly spaced from each neighboring clock edge.

The rejection is based on the contention that "the frequency of the clock is considered to be a design expedient dependent on the particular environment" (Office action at page 2) and "in using the flip flop of Popescu for phase comparison is does not matter which signal is used as the data signal and which is used as the clock signal" (Office action at page 4).

It would not have been obvious to modify Popescu as suggested by the Examiner for several reasons. First, there is no teaching in the art that a lower speed clock should be used. Rather, conventional practice dictates that the speed of the clock be higher than the speed of the data so that all of the transitions of the data will be sampled.

Second, the circuit of Popescu would not operate if modified as suggested by the Examiner. Reversing the data and clock would generate significant asymmetry between the data and

the clock. As a result, the circuit will generate an incorrect phase output signal.

In view of the above, Applicant submits that independent claims 1, 8 and 10 are not obvious in view of Popescu.

Moreover one skilled in the art would not have been motivated to use the circuit of Popescu in the design of a binary phase detector as claimed in claims 1 and 8. See also dependent claims 26 and 37. Popescu is direct to a linear phase detector that generates an output that is proportional to the magnitude of the difference in phase. Claims 1 and 8 are directed to an entirely different class of phase detectors, namely, binary phase detectors. One skilled in the art would not apply the teachings of linear phase detectors to binary phase detector since the two techniques generate significantly different outputs.

The claims that depend on claims 1, 8 and 10 also are patentable over the cited references for the reasons set forth above. In addition, these dependent claims are patentable over the cited references for the additional limitations that these claims contain.

For example, claim 4 relates to the use of low speed and high speed flip flops. The Examiner states on page 5 that this is taught by the flip flops 112 and 113 of Popescu. However, as shown in Figure 2 of Popescu, the data inputs (DIN and DOUT) of the flip flops are of the same frequency. DOUT is merely a retimed version of DIN. Moreover, both flips flops are driven by the same CLK signal. Accordingly, Popescu does not teach or suggest high and low speed flips flops.

Claim 5 recites, in part, "the first flip flop comprises a high speed latch and a low speed latch." The Examiner states that this limitation is taught by conventional master and slave latches. However, conventional master and slave latches are configured to operate at the same speed. Accordingly, this limitation is not taught by the cited references.

Claim 25 recites that the first and second signals are both clock signals. There is no teaching or suggestion to detect a phase difference between two clock signals as claimed in claim 5 (dependent on claim 1).

Also, new claim 24 recites, in part, "each data input provides a lower capacitive load than each clock input so that a lower capacitive load is provided to higher frequency signals than is provided to lower frequency signals." New claim 27 recites, in part, "a signal at the data input of the low speed flip flop is of a lower frequency than the first frequency such that the low speed flip flop is adapted to operate at a lower speed than the high speed flip flop." New claim 28 recites, in part, "the data input of the low speed flip flop provides a lower capacitive load than the data input of the high speed flip flop." New claim 29 recites, in part, "a data input of the low speed latch provides a lower capacitive load than a data input of the high speed latch."

Response to the Rejection of Claims 12, 15, 16 and 19 - 21

Claims 12, 15, 16 and 19 - 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim, U.S. Patent No. 6,388,485 (referred to hereafter as "Kim"), in view of Popescu. Claims 15 and 19 are independent. Claim 12 depends on claim 10.

Kim discloses the use of a binary phase detector in a DLL circuit. See Kim at column 4, lines 15 - 18. For reasons similar to those discussed above, one skilled in the art would not have been motivated to replace the binary phase detector of Kim with a linear phase detector as taught by Popescu. Due to the significant differences in the respective output signals, the combination would not be operable.

Moreover, the rejection of claim 12 is based on the Examiner's contention that all of the limitations of claim 10 are met by Popescu. However, as discussed above, Popescu does teach or suggest the limitations of claim 10. Accordingly, the combination of Kim and Popescu does not teach or suggest all of the limitations of claim 12.

The rejection of independent claims 15 and 19 is based on the Examiner's contention that Popescu discloses the phase detector limitations of claims 15 and 19. As discussed above, however, Popescu discloses a conventional detector circuit where a higher speed signal CLK drives a clock input and a lower speed signal DIN drives a data input. Thus, Popescu does teach or suggest a phase detector where a data input is coupled to a higher speed signal and a clock input is coupled to lower speed signal.

In view of the above, Applicant submits that independent claims 15 and 19 are not obvious in view of Kim and Popescu because the combination of Kim and Popescu does not teach or suggest all of the limitations of either claim 15 or claim 19. Claim 16 that depends on claim 15 and claims 20 - 21 that depend on claim 19 also are patentable over the cited references for the reasons set forth above. In addition, these dependent claims are patentable over the cited references for the additional limitations that these claims contain.

**CONCLUSION**

In view of the above amendment and remarks it is submitted that the claims are patentably distinct over the cited references and that all the rejections to the claims have been overcome. Reconsideration and reexamination of the above application is requested.

Respectfully submitted,
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